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EXAMINER				
FENNEMA, ROBERT E				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/813,615

**Applicant(s)**

KNOWLES, SIMON

**Examiner**

ROBERT E. FENNEMA

**Art Unit**

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 October 2008.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 and 21 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-18 and 21 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-8508)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1-18 and 21 have been considered.

***Claim Objections***

2. The term "substantially equal" in claim 20 is a relative term which renders the claim indefinite. The term "substantially equal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 18 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Hull et al. (USPN 5,922,065, herein Hull)
5. As per Claim 18, Hull teaches: A method of operating a computer processor for processing (i) instruction packets comprising a plurality of only control instructions

(Figure 4, Template "B"); and (ii) instruction packets comprising a plurality of instructions comprising at least one data processing instruction (Figure 4, Template "0"),

the processor comprising a decode unit for decoding sequentially the instruction packets fetched from a memory holding the instruction packets (Column 5, Lines 16-18):

a control processing channels comprising a plurality of functional units (Column 3, Line 51, the branch execution unit) including a control register file having a first bit width (Column 3, Lines 18-21, 64 bits) and a data processing channel comprising a plurality of functional units including a data register file having a second bit width, wider than the first bit width (Column 3, Lines 9-11, the floating point register file has a bit width of 82 bits), the method comprising:

decoding identification bits of each instruction packet to determine which type (i), (ii), of instruction packet is being decoded, and passing the plurality of only control instructions from an instruction packet of type (i) to the control processing channel when the decode circuitry indicates so and passing the plurality of instructions comprising at least one data processing instruction from an instruction packet of type (ii) to the data processing channel when the decode circuitry indicates so (Column 3, Lines 63-66, the template field in each packet/bundle tells the machine what is in each packet, and directs the packet to the appropriate functional units. Template "B" for example contains 3 branch (control) instructions, and Template "0" contains only data-processing instructions);

when the instruction packet defines (i) a plurality of only control instructions, supplying the control instructions to the control processing channel wherein the control instructions are executed sequentially (Column 4, Lines 61-62); and

when the instruction packet defines (ii) a plurality of instructions comprising at least one data processing instruction, supplying at least the data instruction to the data processing channel wherein the plurality of instructions are executed simultaneously (Column 2, Lines 5-9).

6. As per Claim 21, Hull teaches: A computer-readable medium comprising a sequence of instruction packets (Column 2, Lines 22-24),

said instruction packets including a first type of instruction packet comprising a plurality of only control instructions of substantially equal length (Figure 4, Template "B") and a second type of instruction packet comprising a plurality of instructions including at least one data instruction (Figure 4, Template "0"),

said instruction packets including at least one indicator bit at a designated bit location within the instruction packet (Column 3, Lines 63-66, the template fields), wherein the computer-readable medium is adapted to run on a computer such that said indication bit is adapted to cooperate with a decode unit of the computer to designate whether:

a) the instruction packet defines a plurality of only control instructions or a plurality of instructions comprising at least one is a data instruction (Column 3, Lines 63-66); and

b) in the case when there is a plurality of instructions comprising at least one data instruction, the nature of each of the first and second instructions selected from: a control instruction; a data instruction; and a memory access instruction (Figure 4, see Templates "0" or "8" for example).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-7, 11, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, in view of "Unifying FPGAs and SIMD Arrays" by Bolotski et al. (herein Bolotski).

9. As per Claim 1, Hull teaches: A computer processor for processing (i) instruction packets comprising a plurality of only control instructions (Figure 4, Template "B"), and (ii) instruction packets comprising a plurality of instructions comprising at least one data processing instruction (Figure 4, for example, Template "E"), the processor comprising:

a decode unit for decoding sequentially the instruction packets fetched from a memory holding a sequence of instruction packets (Column 5, Lines 16-18);

a control processing channel capable of performing control operations, the control processing channel comprising a plurality of functional units (Column 3, Line 51,

the branch execution unit) including a control register file having a first bit width (Column 3, Lines 18-21, 64 bits); and

a data processing channel capable of performing data processing operation, the data processing channel comprising a plurality of functional units (Column 3, Lines 48-50, the integer, memory, and floating point execution units) including a data register file having a second bit width wider than the first bit width (Column 3, Lines 9-11, the floating point registers have a bit width of 82 bits);

wherein the decode unit comprises decode circuitry configured to decode identification bits of each instruction packet to determine which type (i), (ii) of instruction packet is being decoded, and control circuitry configured to pass the plurality of only control instructions from an instruction packet of type (i) to the control processing channel when the decode circuitry indicates so and to pass the plurality of instructions comprising at least one data processing instruction from an instruction packet of type (ii) to the data processing channel when the decode circuitry indicates so (Column 3, Lines 63-66, the template field in each packet/bundle tells the machine what is in each packet, and directs the packet to the appropriate functional units. Template "B" for example contains 3 branch (control) instructions, and Template "0" contains only data-processing instructions);

wherein, in use the decode unit causes instructions of (i) instruction packets comprising a plurality of only control instructions to be executed sequentially on the control processing channel (Column 4, Lines 61-62); and

wherein in use the decode unit causes instructions of (ii) instruction packets comprising a plurality of instructions comprising at least one data processing instruction to be executed simultaneously on the data processing channel (Column 2, Lines 5-9), but fails to teach:

at least one input of which is a vector.

Hull is silent towards vectors (using the Applicant's definition of a vector in Paragraph 23 of the specification, wherein a vector is an assembly of scalar operands). Hull does however teach that there is a high demand for highly efficient, parallel processing machines, and Bolotski teaches that a massively parallel system of computing is a SIMD processor, which is a vector, or array, of scalar values. Given the disclosed need in Hull of increased parallelism, the teachings of both Bolotski of the parallelism of SIMD (along with SIMD being well known in the art), one of ordinary skill in the art would have been motivated to integrate SIMD processing into the system of Hull, to further exploit parallelism in lines with the goals of Hull.

10. As per Claim 2, Hull teaches: A computer processor according to claim 1, wherein the control processing channel further comprises a branch unit and a control execution unit (Column

11. As per Claim 3, Hull teaches The computer processor according to claim 1, wherein the data processing channel further comprises a fixed data execution unit (Column 3, Lines 48-51), but fails to teach:



the second processing channel containing a configurable data execution unit.

While Hull teaches a fixed data execution unit, Hull is silent towards a configurable data execution unit. However, Bolotski teaches a system that can simulate SIMD and configurable operations on the same unit (Section 4), which can be subdivided until SIMD and configurable units. Boloski further teaches that the advantages of combining a SIMD and configurable unit includes reducing cost by not duplicating logic (Section 4.1), additionally, one of ordinary skill in the art would recognize the additional benefits of configurable hardware, such as being able to configure exactly the units you need, allowing for flexibility and increased performance. Therefore, one of ordinary skill in the art would have been motivated to combine the teachings of Hull and Bolotski to implement configurable data execution units.

12. As per Claim 4, Bolotski teaches: A computer processor according to claim 3, wherein the fixed data execution unit and the configurable data execution unit both operate according to a single instruction multiple data format (Section 4).

13. As per Claim 5, Hull teaches: The computer processor according to claim 1, wherein the control and data processing channels share a load store unit (Column 3, Line 50, there is only one memory execution unit, and since the branch unit needs to be able to have access to memory (to fetch the new target instructions), it clearly has to be shared between the two).

14. As per Claim 6, Hull teaches: A computer processor according to claim 5, wherein the load store unit uses control information supplied by the control processing channel and data supplied by the data processing channel (Column 3, Line 50, there is only one memory execution unit, the data processing channel needs to use it to fetch data from memory, and the control channel needs to use it to fetch branch target addresses).

15. As per Claim 7, Hull teaches: A computer processor according to claim 1, wherein the instruction packets are all of equal bit length (Column 2, Lines 22-24, 128 bit bundles).

16. As per Claim 11, Hull teaches: A computer processor according to claim 7, wherein the nature of each instruction in an instruction packet is selected at least from a control instruction, a data instruction, and a memory access instruction (Column 3, Lines 48-51, also see Figure 4).

17. As per Claim 14, Hull teaches: A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines three control instructions, the decode unit is operable to supply the control processing channel with the three control instructions (Column 3, Lines 65-66) whereby the three control instructions are executed sequentially (Column 4, Lines 61-62).

18. As per Claim 15, Hull teaches: A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines two instructions comprising at least one data instruction, the decode unit is operable to supply the second processing channel with at least the data instruction (Column 3, Lines 65-66) whereby the two instructions are executed simultaneously (Column 2, Lines 5-9).

19. As per Claim 16, Hull teaches: A computer processor according to claim 1, wherein the decode unit is operable to read the values of a set of designated bits at predetermined bit locations in each instruction packet of the sequence (Column 3, Lines 63-66, the template bits), to determine:

a) whether the instruction packet defines a plurality of only control instructions (Figure 4, Template "B") or a plurality of instructions of which at least one is a data instruction (Figure 4, any non-"B" template); and

b) where the instruction packet defines a plurality of instructions of which at least one is a data instruction, the nature of each of the two instructions selected from: a control instruction; a data instruction; and a memory access instruction (Figure 4, see Template "0" or "8" for example).

20. As per Claim 17, Hull teaches: A computer processor according to claim 3, wherein the configurable data execution unit is capable of executing more than two

consecutive operations on the data provided by a single issued instruction before returning a result to a destination register file.

One of ordinary skill in the pertinent art would have recognized that this is a simple accumulate function that would be easily programmable in configurable logic.

21. Claims 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull and Bolotski, in view of In re Rose.

22. These claims recite limitations of the bit lengths of various instructions and packets.

While Hull may not teach the recited lengths, if it was advantageous to lengthen or shorten the bit lengths in Hull for various reasons, one of ordinary skill in the pertinent art would have recognized that it would have been simple to do so.

Further, it has been found that a change in size does not produce a patentable distinction. In re Rose , 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" where held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.).

***Response to Arguments***

23. Examiner notes the Applicant's arguments on Page 3, regarding the general purpose register file, Examiner has apparently misread the paragraph, and Examiner' concedes that the general purpose register file is indeed a 64 bit register file. However, Examiner notes that in the lines below that, it is noted that the floating point register file is an 82 bit register file, and Examiner has interpreted that as the data register file under the currently new grounds of rejection.

24. Applicant has further argued on Page 3 that Hull discloses that all instructions are the same length, however, Examiner does not see how this affects the claim rejections, as there are no limitations as to certain instructions being longer than other instructions.

25. Regarding Claim 21, Applicant argues that Hull does not disclose at least one indicator bit to designate what is in it, and then discloses Hull's template field, but does not specifically indicate why this does not read on the indicator bit. Examiner still believes Hull's template field reads properly on the claim limitation, as the template field is a collection of bits which indicate the contents of the instruction package, one of which could be all control instructions, the others with possible data and/or memory instructions.

26. Regarding Applicant's arguments on Page 5, Applicant has argued that Hull teaches that instructions have the same bit length, and thus teaches away from the claimed invention. However, the claims have absolutely no teaching that the instructions are a different length from one another, and as Applicant has cited the specification in the arguments, instead of any claim language, it appears that the Applicant is attempting to read limitations from the specification into the claims, which is not proper. If this is indeed what Applicant believes differentiates the claims from the prior art, then Applicant is encouraged to incorporate these limitations into the claims, as currently, from the Examiners interpretations of the claims, Claims 1 and 18 requires a data register to have a bit length greater than that of a control register, and Claim 21 has no limitations in regard to any sizing whatsoever. Additionally, if the Applicant can more clearly indicate why the template bits of Hull are not the same as the indicator bit(s) in the claims, it may also be a good direction to move towards to help move the case forward.

27. Examiner believes that the above remarks also address the arguments presented in Page 6 of the remarks.

28. If the Applicant has any questions, Applicant is encouraged to contact the Examiner at the number below.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. FENNEMA whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Friday, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/  
Supervisory Patent Examiner, Art Unit 2183

Robert E Fennema  
Examiner  
Art Unit 2183

RF